What Is Claimed Is:

1. A method of recovering a sequence of data tokens encoded in an analog signal, said method comprising:

receiving said analog signal;

examining said analog signal in analog form for a transition;

capturing a data token by sampling said analog signal, wherein said capturing is performed responsive to said transition;

determining whether to provide said data token as one of said sequence of data tokens; and

if it is determined to provide said data token as one of said sequence of data tokens, providing said data token as said one of said sequence of data tokens.

2. The method of claim 1, said data token is received in said analog signal after said transition.

3. The method of claim 2, wherein each of said sequence of data tokens comprises a bit.

4. The method of claim 3, further comprises generating a first plurality of data tokens by sampling said analog signal at time points specified by a sampling clock signal, wherein said sampling clock signal is generated by examining said analog signal,

wherein said providing comprises selecting said data token generated by said capturing instead of a corresponding one of said first plurality of data tokens.

5. The method of claim 3, further comprises generating said sequence of data tokens based only on data tokens after corresponding transitions such that data tokens are not generated based on a sampling clock generated based on said analog signal.

6. A data recovery circuit for recovering a sequence of data tokens encoded in an analog signal, said data recovery circuit comprising:

means for receiving said analog signal;

means for examining said analog signal in analog form for a transition;

means for capturing a data token by sampling said analog signal, wherein said capturing is performed responsive to said transition;

means for determining whether to provide said data token as one of said sequence of data tokens; and

means for providing said data token as said one of said sequence of data tokens, if it is determined to provide said data token as one of said sequence of data tokens.

7. The data recovery circuit of claim 6, wherein said data token is received in said analog signal after said transition.

8. The data recovery circuit of claim 7, further comprises means for generating a first plurality of data tokens by sampling said analog signal at time points specified by a sampling clock signal, wherein said sampling clock signal is generated by examining said analog signal,

wherein said means for providing selects said data token generated by said capturing instead of a corresponding one of said first plurality of data tokens.

9. The data recovery circuit of claim 7, further comprises means for generating said sequence of data tokens based only on data tokens after corresponding transitions such that data tokens are not generated based on a sampling clock generated based on said analog signal.

10. The data recovery circuit of claim 9, wherein said means for receiving receives said analog signal on a serial communication channel.

11. A data recovery circuit for recovering a sequence of data tokens encoded in an analog signal, said data recovery circuit comprising:

a data transition detector (DTD) circuit detecting a transition in said analog signal;

a sampler circuit sampling said analog signal to generate a sample data token, said sampler circuit sampling said analog signal responsive to the detection of said transition; and

a multiplexor providing said sample data token instead of another data token as one of said sequence of data tokens.

12. The data recovery circuit of claim 11, wherein said sample data token is received after said transition in said analog signal.

13. The data recovery circuit of claim 12, further comprising a recovery circuit

receiving said analog signal and generating a clock-out signal delayed in phase from a sampling clock signal, wherein said sampling clock signal is based on said analog signal.

14. The data recovery circuit of claim 13, wherein said recovery circuit generates said another data token according to said sampling clock.

15. The data recovery circuit of claim 13, wherein said another sample comprises a previous sample, wherein said previous sample is received in said analog signal prior to said sample data token.

16. The data recovery circuit of claim 15, wherein said recovery circuit generates a clock-out clock signal having rising edges approximately at the center of said first plurality of data tokens, said data recovery circuit further comprising:

a second flip-flop receiving a IS_NEW_DATA signal indicating whether present data token generated by said multiplexor is not equal to a data sample presently received on said analog signal, said second flip-flop being clocked by a falling edge of said clock-out clock signal such that said IS_NEW_DATA signal provided on said falling edge as a select signal for said multiplexor; and

a delay block receiving said clock-out clock signal and delaying said clock-out clock signal by an amount equaling propagation delays caused by said second flip-flop and said multiplexor,

said data recovery circuit providing the output of said delay block and the output of said multiplexor as said sequence of data tokens and a corresponding clock signal

respectively.

17. The data recovery circuit of claim 16, wherein each of said sequence of data tokens comprises a bit.

18. A system recovering a sequence of data tokens encoded in an analog signal, said system comprising:

a data recovery circuit for recovering said sequence of data tokens, said data recovery circuit comprising:

a data transition detector (DTD) circuit detecting a transition in said analog signal;

a sampler circuit sampling said analog signal to generate a sample data token, said sampler circuit sampling said analog signal responsive to the detection of said transition; and

a multiplexor providing said sample data token instead of another data token as one of said sequence of data tokens; and

an application block receiving and using said sequence of data tokens.

19. The system of claim 18, wherein said sample data token is received after said transition in said analog signal.

20. The system of claim 19, further comprising a recovery circuit receiving said analog signal and generating a clock-out signal delayed in phase from a sampling clock

signal, wherein said sampling clock signal is based on said analog signal.

21. The system of claim 20, wherein said recovery circuit generates said another data token according to said sampling clock.

22. The system of claim 20, wherein said another sample comprises a previous sample, wherein said previous sample is received in said analog signal prior to said sample data token.

23. The system of claim 22, wherein said recovery circuit generates a clock-out clock signal having rising edges approximately at the center of said first plurality of data tokens, said data recovery circuit further comprising:

a second flip-flop receiving a IS_NEW_DATA signal indicating whether present data token generated by said multiplexor is not equal to a data sample presently received on said analog signal, said second flip-flop being clocked by a falling edge of said clock-out clock signal such that said IS_NEW_DATA signal provided on said falling edge as a select signal for said multiplexor; and

a delay block receiving said clock-out clock signal and delaying said clock-out clock signal by an amount equaling propagation delays caused by said second flip-flop and said multiplexor,

said system providing the output of said delay block and the output of said multiplexor as said sequence of data tokens and a corresponding clock signal respectively.

24. The system of claim 23, wherein each of said sequence of data tokens comprises a bit.